Bergische Universität Wuppertal

Fachbereich Mathematik und Naturwissenschaften

Lehrstuhl für Angewandte Mathematik
und Numerische Mathematik

Lehrstuhl für Optimierung und Approximation

Giuseppe Alì, Andreas Bartel, Markus Brunk, Sebastian Schöps

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Giuseppe Alì[1], Andreas Bartel[2], Markus Brunk[2], and Sebastian Schöps[2]

Abstract A dynamic iteration scheme is proposed for a coupled system of electric circuit and distributed semiconductor (*pn*-diode) model equations. The device is modelled by the drift-diffusion (DD) equations and the circuit by MNA-equations. The dynamic iteration scheme is investigated on the basis of discrete models and coupling via sources and compact models. The analytic divergence and analytic convergence results are verified numerically.

1 Introduction

Distributed semiconductor models result typically in partial differential equations (PDEs). The trend of miniaturization in electronics industry leads to devices of growing complexity, where – due to smaller signals – parasitic effects become more and more important. Description of semiconductor devices by compact models enforces time-consuming parameter fitting and might result in sub-circuits of several hundred parameters for the description of a single device. Thus the coupling of PDE-models and circuit simulation becomes desirable. Efficient techniques to couple the different subsystems are needed. We propose a simple Gauss-Seidel iteration, where the displacement current is explicitly modeled by an extracted capacitance.

In this section the basic models are introduced: for the semiconductor device the drift-diffusion (DD) equations and the surrounding circuit the modified nodal analysis (MNA) equations. In the second section different coupling approaches are discussed. In the third section a dynamic iteration scheme is developed that guarantees unconditional convergence. This is illustrated by a simple numerical example. In the last section we draw some conclusions.

[1]Dipartimento di Matematica, Universitá della Calabria and INFN-Gruppo c. Cosenza, I-87036 Arcavacata di Rende (CS), Italy `g.ali@mat.unical.it`, · [2]Institut für Numerische Analysis, FB C, Bergische Universität Wuppertal, Gaussstrasse 20, 42119 Wuppertal, Germany `{bartel,brunk,schoeps}@math.uni-wuppertal.de`

1.1 Device Model

Our *np*-diode shall be modelled on the domain $\Omega \subset \mathbf{R}^d$ for $d = 1, 2, 3$ with $\partial\Omega = \Gamma = \Gamma_D \cup \Gamma_N$. The DD-model equations consist of conservation laws for the electron and hole densities n, p coupled to the Poisson equation for the electric potential V,

$$\partial_t n - q^{-1}\mathrm{div}\,J_n = -R, \qquad\qquad J_n = \mu_n(U_T \nabla n - n\nabla V), \tag{1a}$$

$$\partial_t p + q^{-1}\mathrm{div}\,J_p = -R, \qquad\qquad J_p = -\mu_p(U_T \nabla p + p\nabla V), \tag{1b}$$

$$\varepsilon_s \Delta V = q(n - p - C(x)), \quad J_{\mathrm{tot}} = \int_{\Gamma_k} \left\{ \varepsilon_s \partial_t \nabla V - (J_n + J_p) \right\} ds. \tag{1c}$$

There $R = R(n, p)$ denotes the generation-recombination term, μ_n, μ_p are the mobility parameters and q the elementary charge. The permittivity is given by ε_s, $C(x)$ is the doping concentration and U_T the thermal voltage. The total current leaving the device at terminal k given by $\Gamma_k \subset \Gamma_D$ is then given by J_{tot} with the displacement current $\varepsilon_s \partial_t \nabla V$. Of course, $k = 1, 2$, and due to charge conservation in the diode, the current is the same for both k.

The model equations are supplemented with initial conditions for n, p and boundary conditions for V, n, p on the Dirichlet boundary Γ_D and for $J_n, J_p, \nabla V$ on the Neumann boundary Γ_N. For the simulations presented below (see §3) we discretized the DD-equations by use of exponentially fitted mixed finite elements as described in [1, 2], since this allows for positivity preservation. Thus the discretized equations can be written in the form

$$A_n d_t \mathbf{n} + B_n \mathbf{n} = f_n(\mathbf{p}, \mathbf{V}), \qquad\qquad L\mathbf{V} = \mathbf{n} - \mathbf{p} - \mathbf{C} + f_V(\mathbf{v}_D), \tag{2a}$$

$$A_p d_t \mathbf{p} + B_p \mathbf{p} = f_p(\mathbf{n}, \mathbf{V}), \qquad\qquad \mathbf{i}_D = j_D(\mathbf{n}, \mathbf{p}, \mathbf{V}), \tag{2b}$$

with regular matrices A_n, A_p, B_n, B_p, L. Here the bold symbols represent the vectors containing the discrete approximations of the corresponding values. $\mathbf{i}_D$ is the discrete approximation of J_{tot} and $\mathbf{v}_D$ denotes the applied voltage drop, which is determined by the surrounding circuit. The boundary conditions are incorporated in the functions f_n, f_p and f_V. We note that standard finite element or finite difference discretization allow for the same representation.

Alternatively the displacement current can be expressed equivalently in terms of the time derivative of the applied voltage drop, [3]; this yields

$$\mathbf{i}_D = C_D \frac{\mathrm{d}}{\mathrm{d}t} \mathbf{v}_D - \mathbf{i}_{SD} \quad \text{with} \quad \mathbf{i}_{SD} := j_{SD}(\mathbf{n}, \mathbf{p}, \mathbf{V}). \tag{2c}$$

For a cubic diode with length l and cross-section A, where a 1d model is sufficient, it holds: $C_D = \frac{\varepsilon_s \cdot A}{l}$.

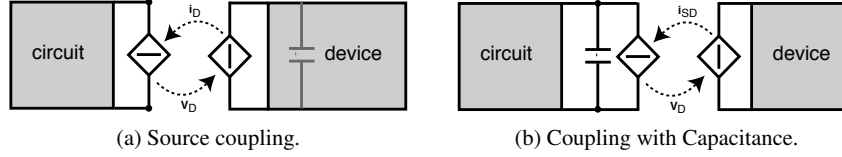(a) Source coupling.   (b) Coupling with Capacitance.

Fig. 1: Coupling with displacement current in device (a) and in circuit (b).

1.2 Circuit model

The extended circuit reads in the flux/charge oriented form of the MNA [4]:

$$A_C \frac{d}{dt}q + A_R g_R(A_R^\top u, t) + A_L i_L + A_V i_V + A_I i(t) + A_D i_D = 0, \qquad (3a)$$

$$\frac{d}{dt}\Phi - A_L^\top u = 0, \qquad\qquad A_V^\top u - v(t) = 0, \qquad (3b)$$

$$q - q_C(A_C^\top u, t) = 0, \qquad\qquad \Phi - \Phi_L(i_L, t) = 0, \qquad (3c)$$

with given functions $q_C(v,t)$, $g_R(v,t)$, $\Phi(i,t)$, $v_S(t)$ and $i_S(t)$ denoting the constitutive relations for charges, resistances, fluxes, voltage and current sources, respectively. Matrices $A_\star$ denote network incidences and i_D is the current through the diode. The unknown of the network are charges $q(t)$, fluxes $\Phi(t)$, node potentials $u(t)$ except ground and currents $i_L(t)$, $i_V(t)$ through inductors and voltage sources.

1.3 Coupling

The structure of the equations allows two representations of the circuit-device coupling: (a) coupling by plain sources (*source coupling*), in which the distributed device model takes the displacement current into account, i.e., i_s is defined by (2b), or, (b) coupling, where the displacement current is described in terms of circuit variables, i.e., (2c) is treated as an additional circuit equation (*coupling with capacitance*), see Fig. 1. In both settings the voltage drop v_D in the circuit is supplied as a boundary condition to the device model. In the case of a monolithic coupling, where all equations are solved in one system, those two representations are equivalent, but in the case of a weak coupling by a dynamic iteration scheme, they exhibit different behavior. – Setting (b) reflects standard compact model design.

Source coupling. Spatial discretization of the DD-equations (2) yields an index-1 DAE (for given $v(t)$) [2]. Assuming the standard loop and cutset conditions, [5], the circuit equations (3) are index-1 as well (for given $i_D(t)$). Assuming the overall system to be of index-1 [6], it can be written in semi-explicit form:

$$\begin{aligned}
\dot{y}_d &= f_d(y_d, z_d), & \dot{y}_c &= f_c(y_c, z_c, z_d), \\
0 &= g_d(y_d, z_d, z_c), & 0 &= g_c(y_c, z_c, z_d),
\end{aligned} \qquad (4)$$

with $\partial \mathbf{g}_d / \partial \mathbf{z}_d$ and $\partial \mathbf{g}_c / \partial \mathbf{z}_c$ regular. The differential variables of the diode and circuit are $\mathbf{y}_d := (\mathbf{n}, \mathbf{p})$ and $\mathbf{y}_c := (\mathbf{q}, \Phi)$, while the algebraic unknowns are $\mathbf{z}_d = (\mathbf{V}, \mathbf{i}_D)$ and $\mathbf{z}_c := (\mathbf{u}, \mathbf{i}_L, \mathbf{i}_V)$. The vector $\mathbf{V}$ describes the space discrete electric potential and $\mathbf{i}_D$ the device current, defined in (1c). Due to spatial discretization the values of $\mathbf{n}, \mathbf{p}$ in some discretization nodes may turn into algebraic variables. This does not pose any problem as long as the index-1 assumptions hold. Thus this case is not considered in the following.

In this setting all node potentials $\mathbf{u}$ are algebraic variables of the circuit and so is $\mathbf{v}_D = \mathbf{A}_D^\top \mathbf{u}$. Hence only $\mathbf{z}_c$ enters the algebraic equations of the device $\mathbf{g}_d$. The diode current is also algebraic, but appears, depending on the circuit's topology, in the differential $\mathbf{f}_c$ and in the algebraic equation $\mathbf{g}_c$ of system (4).

Coupling with Capacitance. Now substituting $\mathbf{i}_D$ by equation (2c) in the current balance equation (3a), we end up with a slightly different system of equations

$$
\begin{aligned}
\dot{\mathbf{y}}_d &= \mathbf{f}_d(\mathbf{y}_d, \mathbf{z}_d), & \dot{\mathbf{y}}_c &= \mathbf{f}_c(\mathbf{y}_c, \mathbf{z}_c, \mathbf{z}_d), \\
\mathbf{0} &= \mathbf{g}_d(\mathbf{y}_d, \mathbf{z}_d, \mathbf{y}_c), & \mathbf{0} &= \mathbf{g}_c(\mathbf{y}_c, \mathbf{z}_c),
\end{aligned}
\tag{5}
$$

with differential unknowns $\mathbf{y}_d := (\mathbf{n}, \mathbf{p})$ and $\mathbf{y}_c := (\mathbf{q}, \Phi, \mathbf{P}_D \mathbf{u})$ and algebraic unknowns $\mathbf{z}_d = (\mathbf{V}, \mathbf{i}_{SD})$ and $\mathbf{z}_c := (\mathbf{Q}_D \mathbf{u}, \mathbf{i}_L, \mathbf{i}_V)$, where $\mathbf{Q}_D$ is a projector onto the kernel of $\mathbf{A}_D^\top$ and $\mathbf{P}_D$ its complement, as typically defined in circuit index analysis, [5]. In this notation the node potentials are split because the capacitance C_D is not written in charge oriented form. The advantages of the charge/flux oriented MNA, i.e., charge conservation, are still respected because of the linearity of C_D.

Due to the capacitive path between the coupling nodes the voltage drop $\mathbf{v}_D$ belongs to the differential variables $\mathbf{y}_c$ and only this enters the device subsystem $\mathbf{g}_d$ and, in turn, the device current $\mathbf{i}_{SD}$ enters only the circuit's differential equation $\mathbf{f}_c$.

2 Dynamic Iteration Schemes

To simulate the coupled system of circuit and discretized device equations efficiently and reliably we propose a dynamic DAE-DAE iteration scheme that ensures stability and speeds up convergence. The key is the coupling via capacitive branches, [7], which is ensured here by fitting the capacitance C_D using the device equations.

In a dynamic iteration scheme, the time interval of interest is split into time windows that are treated sequentially. On these windows, each subsystem is solved independently by a problem-specific time-integrator. The mutual input from the subsystems are considered as a known functions, only dependent on time. The exchange of data between the subsystems is organized in a Gauss-Seidel-like iteration scheme.

The stability and convergence of the iteration depends on the order in which the problems are computed, [8]. For both coupling approaches we may start by computing the diode model or the circuit model first. We will see, that for the coupling with parallel capacitance the iteration will converge, independent of the particular order.

Source coupling. Let us start with the source coupling for the case, that the device is simulated first. The circuit solution $\mathbf{y}_c^{(0)}(t), \mathbf{z}_c^{(0)}(t)$ is considered as known and from that the new device solution $\mathbf{y}_d^{(1)}(t), \mathbf{z}_d^{(1)}(t)$ is obtained. Afterwards the circuit solution $\mathbf{y}_c^{(1)}(t), \mathbf{z}_c^{(1)}(t)$ is updated using the new solution of the device.

$$
\begin{aligned}
\dot{\mathbf{y}}_d^{(1)} &= \mathbf{f}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}), & \dot{\mathbf{y}}_c^{(1)} &= \mathbf{f}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}, \mathbf{z}_d^{(1)}), \\
\mathbf{0} &= \mathbf{g}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}, \mathbf{z}_c^{(0)}), & \mathbf{0} &= \mathbf{g}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}, \mathbf{z}_d^{(1)}),
\end{aligned}
\tag{6}
$$

In this scheme the dependence of the algebraic equation $\mathbf{g}_d$ on the old iterate $\mathbf{z}_c^{(0)}$ will cause divergence, if the contractivity factor α, [8], is too large, that is, if

$$
\alpha = \left\| \left(\frac{\partial \mathbf{g}}{\partial \mathbf{z}^{(1)}} \right)^{-1} \left(\frac{\partial \mathbf{g}}{\partial \mathbf{z}^{(0)}} \right) \right\| > 1, \quad \text{where } \mathbf{g}(\cdot) := (\mathbf{g}_d(\cdot), \mathbf{g}_c(\cdot)), \ \mathbf{z} := (\mathbf{z}_d, \mathbf{z}_c). \tag{7}
$$

A similar contractivity condition occurs for the coupling in reversed order of the subsystems. Clearly the condition vanishes in both orders if the dependence of $\mathbf{g}_d$ on $\mathbf{z}_c$ turns into a differential dependency or $\mathbf{g}_c$ does not depend on the algebraic variable $\mathbf{z}_d$ (for the circuit first), [7]. This is the case for capacitive paths between the device pins and this will be exploited next.

Coupling with Capacitance. In the case of the coupling with parallel capacitances, the contraction factor vanishes regardless of the order of the subsystems. When starting with the device, i.e,

$$
\begin{aligned}
\dot{\mathbf{y}}_d^{(1)} &= \mathbf{f}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}), & \dot{\mathbf{y}}_c &= \mathbf{f}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}, \mathbf{z}_d^{(1)}), \\
\mathbf{0} &= \mathbf{g}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}, \mathbf{y}_c^{(0)}), & \mathbf{0} &= \mathbf{g}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}),
\end{aligned}
\tag{8}
$$

the only dependence on an old iterate in an algebraic constraint is the differential variable $\mathbf{y}_c^{(0)}$ in $\mathbf{g}_d$, hence the contraction factor vanishes. On the other hand, when starting with the circuit subproblem

$$
\begin{aligned}
\dot{\mathbf{y}}_c^{(1)} &= \mathbf{f}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}, \mathbf{z}_d^{(0)}), & \dot{\mathbf{y}}_d^{(1)} &= \mathbf{f}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}), \\
\mathbf{0} &= \mathbf{g}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}), & \mathbf{0} &= \mathbf{g}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}, \mathbf{y}_c^{(1)}),
\end{aligned}
\tag{9}
$$

then there is no dependence on old iterates in algebraic constraints at all; thus again the convergence is unconditional, according to [8].

3 Numerical Results

Next, we visualize the above results by the simulation of a simple series connection of a voltage source, a resistor and an amplified silicon *pn*-diode (1d). The resistance is given as $R = 1\Omega$, the voltage source is given by $v(t) = \sin(\omega t)$V with a frequency
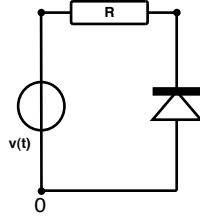
(a) Example circuit

Parameter	Physical meaning	Numerical value
q	elementary charge	$1.6 \cdot 10^{-19}$ As
ε_s	permittivity constant	10^{-10} As/Vm
U_T	thermal voltage at $T_L = 300K$	0.026 V
μ_n/μ_p	low-field carrier mobilities	0.15/0.045 m²/Vs
C_0	maximum doping concentration	10^{23} m⁻³
l	length	10^{-7} m
A	cross-section	10^{-14} m²

(b) Physical parameters for a silicon *pn*-junction diode.

Fig. 2: Circuit and device parameters.

$\omega = 2\pi 10^{11}$ Hz. The diode consists of a 50 nm *n*-region doped with C_0 and a 50 nm *p*-region doped with $-C_0$. The output current of the diode is amplified by the factor 1500, since this causes α (7) to be greater than one. This makes our example on hand rather academic, but on the other hand it illustrates that even in simple setups divergence occurs. Further parameters of the diode are given in Table 2b.

For the following simulations we applied a constant time step size of $\Delta t = 0.1$ps and simulate our circuit und until $T = 10$ ps. On each time window, we accomplish 10 iterations and compare the network variables computed with our dynamic iteration scheme below, to a monolithic reference solution. – The reference solution is made to verify the convergence of the dynamic iteration scheme to the solution of the expensive monolithic systems. Therefore it is computed with same step size.

In the case of circuit first and a parallel capacitance, the algorithm reads:

0) **Initialization.** Set first time window to T_n with $n := 0$.
1) **Guess.** Get a circuit solution $(\mathbf{y}_c^{(0)}, \mathbf{z}_c^{(0)})$ on T_n.
2) **Solve the DAE initial value problems.**
 a) Time-integration of the network on T_n

$$\dot{\mathbf{y}}_c^{(1)} = \mathbf{f}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)}, \mathbf{z}_d^{(0)}), \qquad \text{with } \mathbf{y}_c^{(1)}(t_n) = \mathbf{y}_{c,n}$$
$$\mathbf{0} = \mathbf{g}_c(\mathbf{y}_c^{(1)}, \mathbf{z}_c^{(1)})$$

 b) Time-integration of the circuit on T_n

$$\dot{\mathbf{y}}_d^{(1)} = \mathbf{f}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}), \qquad \text{with } \mathbf{y}_d^{(1)}(t_n) = \mathbf{y}_{d,n}$$
$$0 = \mathbf{g}_d(\mathbf{y}_d^{(1)}, \mathbf{z}_d^{(1)}, \mathbf{y}_c^{(1)}),$$

3) **Sweep Control.** If e.g. $||\mathbf{y}^{(1)} - \mathbf{y}^{(0)}|| >$ tol, then repeat step, i.e., set $(\mathbf{y}_c^{(0)}, \mathbf{y}_d^{(0)}) := (\mathbf{y}_c^{(1)}, \mathbf{y}_d^{(1)})$ and go to Step 2), otherwise Step 4)
4) **Next window.** If $t_{n+1} < T$, then set new initial values $\mathbf{y}_{\star,n+1} := \mathbf{y}_\star^{(1)}(t_{n+1})$ and proceed to the next time window $n := n + 1$, go to Step 1).

In the other cases, the algorithms read analog. – For the numerical comparisons presented below, we replaced the sweep control in the above algorithm by a fix number of ten iteration per time step. In case of reversed order (diode first) or the source
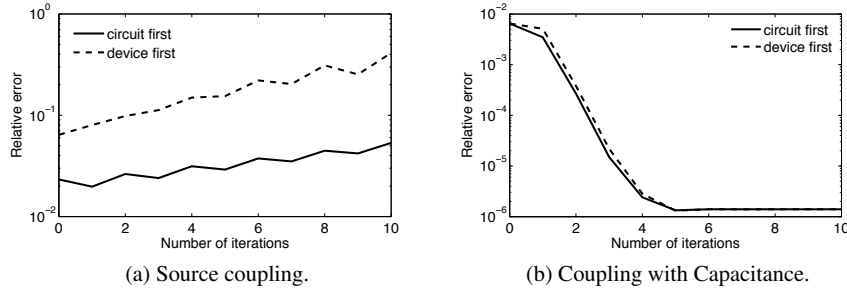
(a) Source coupling.　　　　　　　(b) Coupling with Capacitance.

Fig. 3: Relative error of network components between 2.2–2.3 ps.

coupling approach, the algorithm has been adjusted accordingly.

Source Coupling. First we use the source coupling approach and simulate the simple circuit accordingly. The dynamic iteration scheme does not converge. In Figure 3a we depict the relative error of the network components, i.e. the deviation from the reference solution, against the number of iterations in the time interval 2.2–2.3 ps. We choose this interval, since there simulation breaks down. We clearly see, that for both orders - device or circuit first - the iteration scheme clearly diverges. The different starting values for the two orders is due to bad convergence in the previous time windows and is the result of error propagation. We note, that the amplification of the diode current by the factor 1500 causes the crucial parameter α in (7) to be greater than one, what results in divergence.

Coupling with Capacitance. In the second approach we extract the capacitive behaviour of the diode and model this by a parallel capacitance $C_D = 1.5 \cdot 10^{-14}$ F. In turn, we compute the diode current $\mathbf{i}_{\mathrm{SD}}$ without consideration of the displacement current. In contrast to the source coupling approach, we observe a convergent algorithm. In Figure 3b we depict the relative error (i.e. the relative deviation from the monolithic reference solution) of the network components against the number of iterations in the interval 2.2–2.3 ps, where the source coupling algorithm broke down. We clearly see, that we get convergence with the capacitance in parallel. Moreover, we observed significantly better convergence on the previous time windows, what we easily can deduct from the coinciding starting values for both orders.

Circuit first performs slightly better, which can be physically motivated, since the circuit drives the diode. – Thus the suggested algorithm is coupling with capacitance and circuit first.

4 Conclusion

For PDAE-system occurring for coupled systems of circuits and semiconductor devices dynamic iteration schemes are often based on the source coupling approach. We have shown that even for simple examples this might lead to non-convergent iteration schemes. To overcome this we suggested a dynamic iteration scheme based on the modeling of capacitive effects in semiconductor devices. Capacitive effects are extracted from the device model and modeled by an additional capacitive path in the circuit. We have shown that this approach leads - in accordance with the theory in [8] - to a convergent dynamic iteration scheme independent of the order of computation of the different subsystems. We note that we do not simply add an additional capacitance to the circuit in order to aid convergence, but extract the capacitance from the device model. Thus, it is ensured that the modification does not change our coupled system.

The extracted capacitance can also be regarded as a predictor for the capacitive behavior of the semiconductor device and thus it also can be regarded as a compact model for these effect. Thus, our approach also fits into the framework of [9].

With the suggested coupling via the extracted capacitance we get convergence for both orders – circuit first or device first. However, we observe slightly better convergence for the circuit first approach. We shortly note that this is due to the dependence of g_d on y_c. A deeper analysis of this effect is subject to ongoing research.

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